R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Yamada '537 has been obviated by appropriate amendment and should be withdrawn.

Yamada discloses a message passing system for a distributed shared memory multiprocessor system and a message passing method (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a shared memory and a multiprocessor logic circuit. The shared memory is configured to store data. The multiprocessor logic circuit comprises a plurality of processors and a message circuit. The message circuit is configured to pass messages between the processors. Each of the processors is configured to access the shared memory through a system bus. Claims 12 and 13 provide similar limitations. Yamada does not appear to disclose a system where each of the processors is configured to access a shared memory, as presently claimed.

In particular, the distributed memory shown in FIG. 3 of Yamada (elements 21-1, 21-2 and 21-3) does not appear to be accessible through the so-called system bus (the processor

interconnect 25). For example, the processor 19-1 accesses the memory 21-1 through the processor bus 30-1, not the so-called system bus 25. Similarly, the processor 19-2 accesses the memory 21-2 through the processor bus 30-2, not the so-called system bus 25. Therefore, Yamada does not disclose or suggest **each** of the processors accessing the shared memory through a system bus, as presently claimed.

Furthermore, it is unclear whether the assertion by the Examiner that the memories 21-1, 21-2 and 21-3 are the same as the claimed shared memory is correct. For example, Yamada clearly states in column 6, lines 57-59 that "the processor 19-1 is able to access the distributed shared memory (DSM) 21-1, but is unable to access the other DS memories 21-2 and 21-3". Yamada, by its own explanation, presents a series of distributed memories that are not the same as the claimed shared memory configured to be accessed by each of a plurality of processors. The various distributed memories of Yamada are not accessible as presently claimed. For example, if the distributed memories 21-1, 21-2 and 21-3 are considered to be a single memory (as asserted in the Office Action), then **each** of the processors 19-1, 19-2 and 19-3 are not able to access the distributed memory of Yamada. In particular, the processor 19-1 is unable to access the distributed memories 21-2 and 21-3. The lack of accessing the distributed memory is consistent with Yamada's disclosure of distributing a memory. The

lack of accessing the distributed memory is not consistent with the presently claimed invention that is concerned with providing a shared memory that is accessible by each of a plurality of processors. Therefore, Yamada does not disclose or suggest each and every element of the claimed invention and the rejection should be withdrawn.

Dependent claims 2-11 and 14-20 depend, directly or indirectly, from the independent claims, which are now believed to be allowable.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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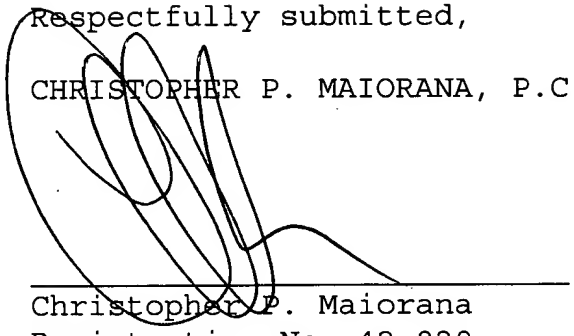

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